Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1.-16. (Canceled)

Please add the following new claims:

17. (New) A content addressable memory having a function for extending a data width, comprising:

a plurality of memory blocks each having a plurality of CAM words, the plurality of memory blocks are divided into the same number of physical segments as maximum number of combinable words to form an entry;

entry configuration set means for setting the number of CAM words which are combined to form an entry, arranged outside each memory blocks; and

a logical-segment-to-physical-segment converting circuit for converting logical-segment-to-be searched signal that indicates a position of words to be searched to the physical-segment-to-be-searched instruction signal according to the setting of said entry configuration set means.

18. (New) A content addressable memory according to claim 17, wherein said entry configuration set means is capable of setting the number of words which is a divisor of the maximum number of words which are combined, where the divisor includes 1 and the maximum number of words which are combined.

19. (New) A content addressable memory according to claim 18, wherein said entry configuration set means is a register.

20. (New) A content addressable memory according to claim 19, wherein the register is a register having a bit width corresponding to the number of said physical segments.

21. (New) A content addressable memory according to claim 17, wherein the physical segments each comprise:

a search bit line;

a search bit line driver for driving the search bit line according to search data; and

a plurality of one-word circuits, each stores the data of one word and which are searched for a match between the stored data and the search data driven on the search bit line to output a search result.

22. (New) A content addressable memory according to claim 21, wherein said entry configuration set means is capable of setting the number of words which is a divisor of the maximum number of words which are combined, where the divisor includes 1 and the maximum number of words which are combined.

23. (New) A content addressable memory according to claim 22, wherein said entry configuration set means is a register.

24. (New) A content addressable memory according to claim 23, wherein the register is a register having a bit width corresponding to the number of said physical segments.

25. (New) A content addressable memory according to claim 22, wherein each of the one-word circuits includes a CAM word having a plurality of CAM cells, and word logic for processing the search result output from the CAM word;

the word logic includes a match flag register for holding the search result,

an AND chain for processing the match flag data of the plurality of words coupled to each other in an entry; and

an entry match output circuit for outputting a match flag for the entry.

26. (New) A content addressable memory according to claim 25, each of the physical segments further including a match flag control signal generating circuit for generating a match flag control signal which is a timing signal for capturing and holding the search result output from the one-word circuit.

27. (New) A content addressable memory according to claim 26, wherein, when search operation is executed, only the search bit line in a physical segment to be searched is driven by the search bit line driver.

28. (New) A content addressable memory according to claim 27, wherein said entry configuration set means is a register.

29. (New) A content addressable memory according to claim 28, wherein the register is a register having a bit width corresponding to the number of said physical segments.

30. (New) A content addressable memory having a function for storing a plurality of entries composed of a combination of a plurality of words and searching for each word of the entries, comprising:

a plurality of memory blocks each having a plurality of CAM words, and the plurality of memory blocks are divided into the same number of physical segments as maximum number of combinable words to form an entry;

entry configuration set means for setting the number of CAM words which are combined to form an entry, arranged outside each memory blocks; and

a logical-segment-to-physical-segment converting circuit for converting logical-segment-to-be searched signal that indicates a position of words to be searched to the

physical-segment-to-be-searched instruction signal according to the setting of said entry configuration set means.

31. (New) A content addressable memory according to claim 30, each physical segment including:

a search bit line;

a plurality of one-word circuits each stores the data of one word and are searched for a match between the stored data and search data driven on the search bit line to output a search result; and

a search bit line driver for driving the search bit line according to the search data.

32. (New) A content addressable memory according to claim 31, wherein, said entry configuration set means outputs entry representative physical segment instruction signal to each physical segment according to the setting of the entry configuration, and after search operation for one or more words within an entry is executed, search result output from the one-word circuit in the representative physical segment is search result of the entry.

33. (New) A content addressable memory according to claim 32, the word having the smallest address or the largest address within an entry is designated as representative word of the entry.

34. (New) A content addressable memory according to claim 32, said logical-segment-to-physical-segment converting circuit output physical segment to be searched instruction signal to each physical segment, and physical segment instructed to search only executes search operation.

35. (New) A content addressable memory according to claim 34, wherein each of the one-word circuits includes a CAM word having a plurality of CAM cells, and word logic for processing the search result output from the CAM word; the word logic further includes:

a match flag register for holding the search result;

an AND chain for processing the match flag data of the plurality of words coupled to each other in an entry; and

an entry match output circuit for outputting a match flag for the entry.

36. (New) A content addressable memory according to claim 35, wherein the CAM cells are mismatch-detection type CAM cells.